

## Refine Search

### Search Results -

Terms	Documents
L1 same multiple same (empt\$3 or free)	5

**Database:**

US Pre-Grant Publication Full-Text Database  
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**Search:**

L2

Refine Search

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Interrupt

### Search History

DATE: Wednesday, April 12, 2006   [Printable Copy](#)   [Create Case](#)

**Set Name Query**

side by side

*DB=PGPB; PLUR=YES; OP=OR***Hit Count Set Name**

result set

<u>L2</u>	L1 same multiple same (empt\$3 or free)	5	<u>L2</u>
<u>L1</u>	synchronous\$3 same asynchronous\$3 same (rate or speed)	1790	<u>L1</u>

END OF SEARCH HISTORY

## Refine Search

### Search Results -

Terms	Documents
L4 and bridge	0

Database:

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Search:

L6

Refine Search

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#### Set Name Query

side by side

#### Hit Count Set Name

result set

DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L6   L4 and bridge

0   L6

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L5   L4 and bridge

31   L5

L4   L1 same multiple

231   L4

L3   L1 same multiple same (empt\$3 or free)

5   L3

DB=PGPB; PLUR=YES; OP=OR

L2   L1 same multiple same (empt\$3 or free)

5   L2

L1   synchronous\$3 same asynchronous\$3 same (rate or speed)

1790   L1

END OF SEARCH HISTORY

## Refine Search

### Search Results -

Terms	Documents
(375/354  370/230  370/232  370/235  370/401  370/402  709/253  710/306  710/310  710/311  710/52  710/53  710/100  710/33  710/307  340/2.1  712/29  713/322  713/501  713/600).ccls.	16596

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Search:






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Set

Name Queryside by  
side

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L7 710/306,310,311,52,53,100,33,307;713/322,501,600;712/29;709/253;375/354;370/230,232,235,401,402;340/2.1

DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L6 L4 and bridge

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L5 L4 and bridge

L4 L1 same multiple

L3 L1 same multiple same (empt\$3 or free)

DB=PGPB; PLUR=YES; OP=OR

L2 L1 same multiple same (empt\$3 or free)

L1 synchronous\$3 same asynchronous\$3 same (rate or speed)

END OF SEARCH HISTORY

## Refine Search

### Search Results -

Terms	Documents
L5 and L7	2

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Search:

L8





### Search History

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SetName Query

side by side

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L8 L5 and L7L7 710/306,310,311,52,53,100,33,307;713/322,501,600;712/29;709/253;375/354;370/230,232,235,401,402;340/2.1

DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L6 L4 and bridge

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L5 L4 and bridgeL4 L1 same multipleL3 L1 same multiple same (empt\$3 or free)

DB=PGPB; PLUR=YES; OP=OR

L2 L1 same multiple same (empt\$3 or free)L1 synchronous\$3 same asynchronous\$3 same (rate or speed)

END OF SEARCH HISTORY



**EAST - [Untitled1:1]**

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☐ Drafts  
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☒ Active  
     L1: (4326) synchronous\$  
     L2: (5) 11 same multip  
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☐ Saved  
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☐ Tagged (0)  
☐ UDC  
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11 same multiple same empty\$3

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	U	I	Document ID	Issue Dat	Pages	Title	Current OR	Current XR
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6990598 B2	20060124	16	Low power reconfigurable systems	713/600	713/322; 713/500
2	<input type="checkbox"/>	<input type="checkbox"/>	US 6289065 B1	20010911	43	FIFO status indicator	375/372	375/371; 711/155
3	<input type="checkbox"/>	<input type="checkbox"/>	US 5450549 A	19950912	21	Multi-channel image array buffer and switch	345/556	345/531; 345/558;
4	<input type="checkbox"/>	<input type="checkbox"/>	US 5258725 A	19931102	13	Phase lock loop with compensation for voltage	331/17	331/25
5	<input type="checkbox"/>	<input type="checkbox"/>	US 4839640 A	19890613	40	Access control system having centralized/dist	340/5.33	235/382; 340/3.51;



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IEEE JNL	IEEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEEE CNF	IEEE Conference Proceeding
IEEE STD	IEEE Standard

- ☐ 1. **The desk area network**  
 McAuley, D.R.; Leslie, I.M.;  
[Electronics & Communication Engineering Journal](#)  
 Volume 9, Issue 3, June 1997 Page(s):143 - 152  
[AbstractPlus](#) | Full Text: [PDF](#)(1592 KB) [IEEE JNL](#)
- ☐ 2. **Memory faults in asynchronous microprocessors**  
 Lloyd, D.W.; Garside, J.D.; Gilbert, D.A.;  
[Advanced Research in Asynchronous Circuits and Systems, 1999. Proceedings. Fifth International Symposium on](#)  
 19-21 April 1999 Page(s):71 - 80  
 Digital Object Identifier 10.1109/ASYNC.1999.761524  
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## Memory faults in asynchronous microprocessors

Lloyd, D.W., Garside, J.D., Gilbert, D.A.

Dept. of Comput. Sci., Manchester Univ., UK;

This paper appears in: **Advanced Research in Asynchronous Circuits and Systems, 1999. Proceedings., Fifth International Symposium on**

Publication Date: 19-21 April 1999

On page(s): 71 - 80

Number of Pages: xii+251

Meeting Date: 04/19/1999 - 04/21/1999

Location: Barcelona

INSPEC Accession Number: 6415609

Digital Object Identifier: 10.1109/ASYNC.1999.761524

Posted online: 2002-08-06 22:28:48.0

## Abstract

Although a large number of **asynchronous** microprocessors have now been designed, relatively few have attempted to handle memory faults. Memory faults create problems for the design of any pipelined system which are exacerbated by the non-deterministic nature of an **asynchronous** processor. This paper describes these problems as encountered in the design of **asynchronous** ARM processors and discusses their specific solutions in the AMULET3 processor. Different mechanisms were used, as expedient, to maintain coherency for the various state-holding elements within the processor; these include register renaming and history buffering in addition to resource locking

## Index Terms

## Inspec

## Controlled Indexing

asynchronous circuits buffer storage microprocessor chips pipeline processing

## Non-controlled Indexing

AMULET3 processor ARM processors asynchronous microprocessors history buffering memory faults pipelined system register renaming resource locking

## Author Keywords

Not Available

## References

No references available on IEEE Xplore.

## Citing Documents

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